Attorney Docket No. : ROC920030301US2
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Luick, David** For: **"Adaptive thread ID cache mechanism for autonomic performance tuning"**	Customer Number: **25854**

AFFIDAVIT PURSUANT TO 37 C.F.R. 1.131

1. My name is David A. Luick. I am over twenty-one years old and I make the following declaration based on my own personal knowledge.

2. I am the inventor of the invention disclosed and claimed in the above-referenced patent application, which I have assigned to IBM Corporation (hereinafter "IBM").

3. I conceived and reduced to practice the above-referenced invention as part of my work for IBM in Rochester, Minnesota, by no later than March 31, 2003. This is evidenced by the document entitled "Disclosure ROC8-2003-0305" attached hereto as Exhibit A.

4. The document shown in Exhibit A is a standard IBM invention disclosure form. It contains a complete disclosure of the invention claimed in the present application.

5. Upon reducing the invention to practice, I completed this invention disclosure document and submitted it to the IBM Office of Counsel, Intellectual Property Law on March 31, 2003. This is also evidenced in Exhibit A.

6. Typically, invention disclosure submissions at IBM go through a review process in which an invention disclosure team (IDT) reviews a disclosure to determine if it meets IBM's criteria for pursuing patent protection. Because of the number of tasks involved in the review and the case load at IBM, this review typically takes several months.

7. The review for the disclosure in Exhibit A was completed on July 24, 2003 and the evaluation was entered by the leader of the IDT on July 25, 2003. This is also evidenced in Exhibit A.

8. If the IDT recommends pursuing patent protection for the disclosed invention, then the IBM Office of Counsel, Intellectual Property Law makes a final decision on whether to pursue the application and, if the decision is to pursue patent protection, it transmits a copy of the disclosure to a patent attorney or agent to prepare the patent application.

9. The final decision in the present case was made on August 4, 2003 and the disclosure was sent to Bryan W. Bockhop, Esq. on that date. This is evidenced in a letter sent to Mr. Bockhop on that date, attached hereto as Exhibit B.

10. U.S. Patent Application No. 10/670,717, of which the present application is a divisional application, was subsequently filed on September 25, 2003.

11. Each responsible person was diligent in pursuing patent protection for this invention at each stage of the disclosure approval process and the patent application preparation and filing process.

I declare under penalty of perjury that the foregoing is true and correct.

May 4, 2007
Date

David A. Luick

Exhibit A

Disclosure ROC8-2003-0305

Prepared for and/or by an IBM Attorney -

Created By Dave Luick On 03/13/2003 02:24:03 PM EST
Last Modified By Enterprise Agentmgr On 08/04/2003 11:14:54 AM EDT

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

***Title of disclosure (in English)**
Adaptive Thread ID Cache Mechanism for Autonomic Performance Tuning

Summary

Status	Final Decision (File)
Final Deadline	
Final Deadline Reason	
Docket Family	ROC9-2003-[redacted]
*Processing Location	Rochester
*Functional Area	select [redacted]
Attorney/Patent Professional	Robert Williams/Rochester/IBM
IDT Team	select [redacted]Rochester/IBM [redacted]/Rochester/IBM [redacted]/Rochester/IBM [redacted]Rochester/IBM [redacted]Rochester/IBM [redacted]/Rochester/IBM [redacted]/Rochester/IBM [redacted]Rochester/IBM [redacted]Rochester/IBM [redacted]i/Rochester/IBM [redacted]/Rochester/IBM [redacted]Rochester/IBM [redacted]/Rochester/IBM
Submitted Date	03/31/2003 06:40:05 PM EST
*Owning Division	[redacted]
Incentive Program	
Lab	
*Technology Code	[redacted]
PVT Score	[redacted]

Inventors with a Blue Pages entry

Inventors: Dave Luick/Rochester/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
> Luick, David A.	[redacted]			

> denotes primary contact

Exhibit A

Main Idea for Disclosure ROC8-2003-0305

Prepared for and/or by an IBM Attorney -

Archived On 07/26/2003 12:02:23 AM

Title of disclosure (in English)
Adaptive Thread ID Cache mechanism for autonomic performance tuning

Main Idea of disclosure
1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.
The problem to be solved is that L1 Caches are unable to implement the high set associativity required when executing in a simultaneous multithreading execution mode without significant costs in area,power,additional access latency,and significant redesign resource and schedule.

2. Summary of Invention: Briefly describe the core idea of your invention (saving the details for questions #3 below). Describe the advantage(s) of using your invention instead of the known solutions described above.
Invention temporarily uses a thread ID bit(s) to divide up an L1 Cache to inhibit thrashing and simulate the performance of 2X(or more) associativity.

3. Description: Describe how your invention works, and how it could be implemented, using text, diagrams and flow charts as appropriate.

Figure 1 shows a basic implementation of a set associative data cache where going from 2-way to 4- or 8-way set associative will significantly lengthen the cycle time or add a cycle of delay of a high frequency (≤10 F04 inverter delays/cycle) pipelined cache. The extra late select width design of the cache array slows it considerably, as well as growing the area and wire delay of the cache array and associated directory. Further, it is also desirable to add multithreading to an existing cache design without requiring substantial modification to the base design.

Figure 2 shows the baseline scheme of the invention where one (or more) of the cache address index bits can alternately be taken from the effective address adder or from the thread identifier bit(s) under control of a special control bit (MSR bit) available to software. A two-way set associative cache will often times exhibit very extensive thrashing when two (or more) threads are simultaneously executing out of a small L1 cache, especially if one of the threads is streaming in array and/or vector elements at a very high rate.

For these situations, which may only be temporary or semipermanent, performance can be greatly improved by eliminating most of the thrashing by temporarily dividing the cache into multiple portions, one portion for each active thread. Dividing a cache into two halves doubles the effective overall associativity as each half now wraps around separately and each sees two independent sets as opposed to two threads seeing a 2X unified cache at two sets total.

Figure 3 shows an adaptive or autonomic control feature for dynamically controlling when the thread ID bit (or bits) is to be used to effectively split the cache.

Figure 3A shows a simple scheme which simply detects when both threads are actively executing, defined as neither having a demand cache miss being satisfied by main memory, and one of them being a streaming thread as identified as a second bit of thread ID, a streaming ID bit.

Exhibit A

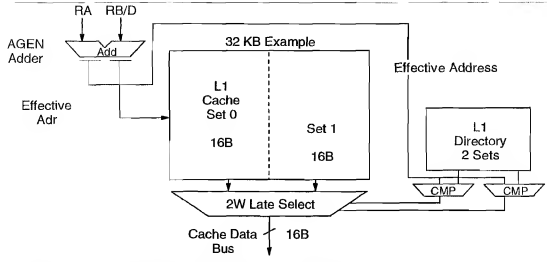
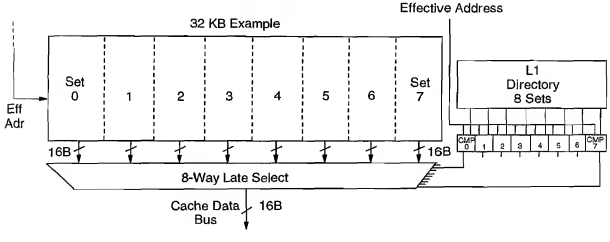


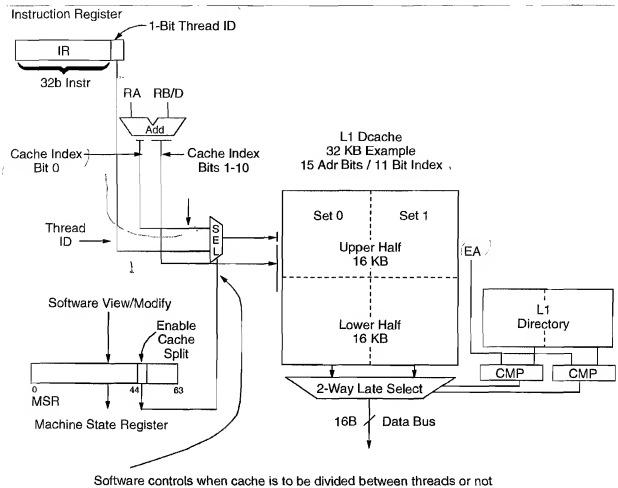
Figure 1A. 2-Way Set Associative Example



DLUI002.PRZ--1

Figure 1B. 8-Way Set Associative Example

4X wires, 2X power, 1.4X area, 1.2X delay
4X late select is very expensive



DLUI002.PRZ-2

Figure 2. Base Invention Scheme

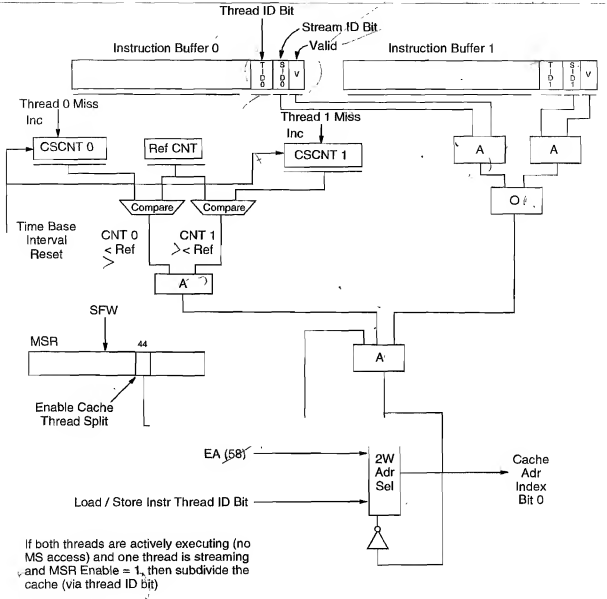
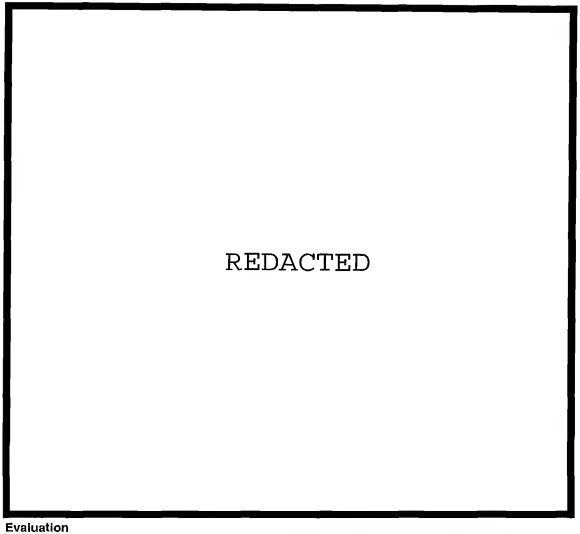


Figure 3. Adaptive Autonomic Control



Evaluation

This evaluation was entered by [redacted]/Rochester/IBM on 07/25/2003

Team Evaluation
What is the team's evaluation of this disclosure? Search
Date rated : 07/24/2003
Evaluation Comments Board rates search. This is especially valuable when used in a chip which has high volumes such as a processor for a game machine.

Final Evaluation History	Who made the final evaluation	Final evaluation date
Search	[redacted]/Rochester/IBM	7/24/2003

Search Information

Date sent:	*Target completion date:	Search Results Received date:
Who was the search sent to (This area is to designate a Local Searcher name or WAIPL):		
*Search Type: ☐ Patentability ☐ Clearance ☐ Validity ☐ State of Art		

Exhibit A

*Features to be searched:

Search Office Information

Target completion date:	☐ Search has been delayed	Ship/Return date:
Search Conducted By		
Comments		

Final Decision

This decision was entered by [redacted]/Rochester/IBM on **08/04/2003**

Decision: File	Status: N/A
PPM Area: 200 - Computer and Processor Architecture	Attorney Rating: [redacted]
Date of Final Decisic... 08/04/2003	

Additional filing information

Planned Filing date: 09/15/2003

Filing comments: This patent application will be prepared by outside counsel, Bryan Bockhop. He will contact you directly regarding this patent application.

Additional decision comments

Bar Date for Autonomic Computing Incentive Award is 09/30/03.

Final Decison History

Entered on 4-Aug-2003 by [redacted]
File N/A 4-Aug-2003 Docket Family: [redacted]

Post Disclosure Text & Drawings

To add additional information related to this disclosure once it has been submitted, click the action button below and a new document will be opened for you to enter the new information. To view existing post disclosure information, double-click on the item in the list below (if there has been additional information entered), and the document will open for you to view.

Date entered **Post disclosure information (comments and drawings)**

Form Revised 09/01/02)

IBM **Exhibit B**

3605 Highway 52 N
Rochester, MN 55901

Office of Counsel,
Intellectual Property Law
voice 507-253-2761
fax 507-253-2382

August 04, 2003

Bryan W. Bockhop
Arnall, Golden & Gregory, LLP
2800 One Atlantic Center
1201 West Peachtree Street
Atlanta, GA 30309-3450

Subject: IBM Patent Application - Docket ROC920030301US1
"Adaptive Thread ID Cache Mechanism for Autonomic Performance Tuning"

INCENTIVE AWARD BAR DATE: September 30, 2003

Dear Bryan:

Enclosed, please find a copy of the original invention disclosure ROC82003-0305 and the inventor information sheet for the subject IBM docket. We would like you to prepare a patent application for this invention by the **Work Plan Date** of **September 15, 2003**, and limit preparation costs to [redacted]

Please feel free to call me with any comments or questions you may have.

Sincerely,

REDACTED

for [redacted] Patent Agent
Intellectual Property Law

[redacted]

Enclosures

PREPARED BY IP LAW